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February 3, 2000

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## Box Patent Application

Assistant Commissioner for Patents  
Washington, DC 20231

Presented for filing is a new patent application claiming priority from a provisional patent application of:

Applicant: MICHAEL LOECHNER

Title: 4-20 MA INTERFACE CIRCUIT

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	<u>Pages</u>
Specification	6
Claims	3
Abstract	1
Declaration	[To be Filed at a Later Date]
Drawings	9

Enclosures:

— Postcard.

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60,118,347, filed February 3, 1999.

Basic filing fee	\$690
Total claims in excess of 20 times \$18	\$0
Independent claims in excess of 3 times \$78	\$0
Fee for multiple dependent claims	\$0
Total filing fee:	\$690

No filing fee is being paid at this time. Please apply any other required fees, **EXCEPT FOR THE FILING FEE**, to deposit account 06-1050, referencing the attorney document number shown above. A duplicate copy of this transmittal letter is attached.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (202) 783-5070.

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Page 2

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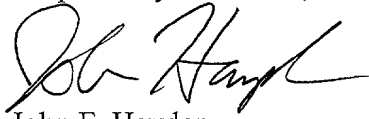
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Respectfully submitted,

A handwritten signature in black ink, appearing to read "John F. Hayden". The signature is fluid and cursive, with the first name "John" and last name "Hayden" clearly distinguishable.

John F. Hayden

Reg. No. 37,640

Enclosures

JFH/kxm

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**APPLICATION FOR  
UNITED STATES PATENT**

**in the name of**

**Michael Loechner**

**for**

**4-20 mA Interface Circuit**

# 4-20 mA Interface Circuit

## CROSS REFERENCE TO RELATED APPLICATION

This application claims priority from U.S. Provisional Application No. 60,118,347, which was filed on February 3, 1999, and is incorporated by reference.

## TECHNICAL FIELD

This invention relates to industrial control systems, and more particularly to a circuit for interfacing with a pair of wires that provides the circuit with power, an analog current control signal, and bi-directional digital communications.

## BACKGROUND

In industrial control systems, it is known to control an instrument, such as a valve controller, using a 4-20 mA DC signal supplied by a control system on a single pair of wires. Typically, the single pair of wires also provides electrical power to the instrument.

It is also known to superimpose bi-directional digital communications signals on the pair of wires. To achieve such communications, the instrument may include a variable impedance line interface circuit that maintains a low impedance at frequencies below 25 Hz to accommodate 4-20 milliamp analog signal variations without substantial terminal voltage fluctuation while also maintaining a substantially higher and relatively constant impedance across the frequency band (e.g., 500-5000 Hz) used for the digital communications.

The HART protocol is one known protocol for providing a 4-20 mA analog control signal in conjunction with bi-directional digital communications. The HART protocol achieves simultaneous analog and digital transmission by using a frequency shift keying (FSK) method to overlay a bi-directional digital signal on the analog control signal.

## SUMMARY

In one general aspect, the invention features a 4-20 mA input interface circuit for communicating with a two-wire loop. The interface circuit includes a power extraction circuit connected to the two-wire loop and operable to generate a DC operating voltage for use in powering the interface circuit and a related device. The power extraction circuit

includes a DC-to-DC converter that generates the DC operating voltage as a voltage having a smaller magnitude than a voltage between the two wires of the two-wire loop. The interface circuit also includes a current sensor connected to the two-wire loop and operable to generate a measure of an analog current through the two-wire loop, the measure being used in

controlling a device associated with the interface circuit. Finally, the interface circuit includes a digital communications circuit connected to the two-wire loop and operable to inject a digital transmission signal on to the two-wire loop and to extract a digital reception signal from the two-wire loop. The digital communications circuit includes an impedance controller having an operational amplifier connected to control an impedance presented to the two-wire loop by the interface circuit.

Embodiments may include one or more of the following features. For example, the impedance controller may be operable to present a stable impedance to the two-wire loop for frequencies in a digital communications band that may extend, for example, from 500 Hz to 10 kHz. The impedance controller also may present an impedance substantially less than the stable impedance for frequencies outside of the digital communications band. The impedance in the digital communications band may be between 200 and 300 ohms, and may be, for example, 250 ohms.

The impedance controller may be operable to inject the digital transmission signal without reducing the impedance substantially below the stable impedance. This permits the interface circuit to operate without separate modes for transmission and receipt of digital communications signals.

The impedance controller may include a filter connected to one or more inputs of the operational amplifier.

In another general aspect, the invention features a valve controller having a 4-20 mA interface circuit having terminals for connection to a two-wire loop, a processor in data communication with the interface circuit and operable to generate a control signal for controlling a valve position, and a control device operable to control the valve position in response to the control signal from the processor. The 4-20 mA interface circuit includes a power extraction circuit connected to the two-wire loop and operable to generate a DC operating voltage for use in powering the interface circuit and the processor, a current sensor connected to the two-wire loop and operable to generate a measure of an analog current through the two-wire loop, the measure being used in controlling a device associated with the

interface circuit, and a digital communications circuit connected to the two-wire loop and operable to inject a digital transmission signal on to the two-wire loop and to extract a digital reception signal from the two-wire loop. The digital communications circuit includes an impedance controller having an operational amplifier connected to control an impedance presented to the two-wire loop by the interface circuit.

Other features and advantages will be apparent from the description and drawings, and from the claims.

### DESCRIPTION OF DRAWINGS

Fig. 1 is a block diagram of a system including a valve controller.

Fig. 2 is a block diagram of the valve controller of the system of Fig. 1.

Fig. 3 is a block diagram of input circuitry of the valve controller of Fig. 2.

Fig. 4 is a graph of frequency characteristics of the input circuitry of Fig. 3.

Figs. 5-10 are circuit diagrams of the valve controller of Fig. 2.

### DETAILED DESCRIPTION

Fig. 1 illustrates a system 100 including a valve controller 105 that includes a 4-20 mA interface circuit. As shown, the valve controller 105 receives a set value ( $w$ ) from a two-wire control loop 110, with the set value ( $w$ ) being in the form of an analog current that varies between 4 and 20 mA. The system 100 also may include, for example, a transmitter 115 and a master controller 120.

The valve controller 105 generates a pneumatic pressure that controls a valve 125. The set value ( $w$ ) supplied to the valve controller indicates the desired position of the valve. The pneumatic pressure generated by the valve controller determines the position of the valve 125. The position of the valve 125 is, in turn, sensed by the valve controller 105, which compares the desired valve position (as indicated by set value  $w$ ) to the actual valve position, and adjusts the pneumatic pressure accordingly until the two match. In some implementations, a separate pneumatic actuator may interconnect the valve controller and the valve.

Fig. 2 provides a more detailed block diagram of the valve controller 105. As shown, an input circuit 200 provides an interface between the two-wire loop 110 and a microprocessor 205. The microprocessor 205 also receives a position signal from a position converter 210, which is a device that is mechanically connected to the valve 125 and which

converts the position of the valve into an electrical signal. For example, the position converter 210 may be a potentiometer having an electrical resistance that varies with the position of the valve. The microprocessor 205 implements an algorithm that processes the set value signal from the two-wire loop and the position signal to produce a control signal  
5 supplied to a current-to-pressure (“I/P”) transducer 215.

The I/P transducer 215 converts the control signal from the microprocessor into air at a pressure proportional to the control signal. This pressurized air is supplied to a preamplifier 220 to increase its pressure, and from there passes to a booster 225 to increase its volume. Both the preamplifier and the booster receive supply air s at, for example, 20-90  
10 psig from a supply line 230. The pneumatic pressure at the output of the booster is supplied to the actuator 120.

The valve controller 105 may optionally include pressure sensors 235, 240. Pressure sensor 240 monitors the pressure at the output of the booster 225, and pressure sensor 235 monitors the pressure from the supply line 230. The respective electrical outputs of the  
15 pressure sensors are provided to the microprocessor, which uses them in diagnostic testing of one or more of the valve controller 105 and the valve 125.

Fig. 3 illustrates the input circuit 200 of the valve controller 105 in more detail. As shown, Loop+ and Loop- designate, respectively, the terminal connections 300, 305 to the two-wire control loop.

Power for the valve controller 105 is extracted from the control loop using circuitry including a DC-to-DC converter 310. The converter 310 provides a 3:1 reduction in the loop voltage, which is typically on the order of 10 Volts. A diode 312 rectifies the input to the converter 310 and to an oscillator 314. The oscillator 314 controls the converter 310 to provide a fixed, 3 Volt supply voltage 316 (Vcc) for use by other components of the  
20 controller 105.

The analog control current on the control loop is monitored by a 21 Ohm measurement resistor 320 that produces a voltage proportional to the loop current. A bridge circuit 322 and a filter 324 provide this voltage to an analog-to-digital converter 326 that converts the voltage to a digital value for use by the microprocessor 205.

Bi-directional digital communications are handled by the combination of a HART modem 330 and an impedance controller 335. For the reception of digital communications signals, the HART modem 330 includes a filter 340 that detects high frequency FSK  
30

variations in the loop current. When these variations, which typically have magnitudes on the order of 1 mA, are detected, the modem 330 converts frequency content of the variations in to a digital reception signal (RxD) and generates a communications interrupt (ComInt\*). The modem then supplies both of these signals to the microprocessor 205.

5       The HART modem 330 initiates transmission of a digital signal in response to a request to send signal (Rts) and a digital packet (TxD) describing the desired transmission from the microprocessor 205. In particular, the HART modem 330 transmits a signal (Tx) to the impedance controller 335 in the form of a 0.25 V FSK AC signal in combination with a 0.25 V DC offset such that the signal Tx varies between 0 and 0.5 V.

10       The impedance controller 335 provides an impedance on the order of 250 Ohms in the digital signaling spectrum, which extends from 500 Hz to 10 kHz. The impedance drops quickly for frequencies below 500 Hz and greater than 10 kHz. This permits the input circuit to present the signal attenuation characteristics illustrated in Fig. 4.

15       The impedance controller 335 includes a filter 350 that acts as the input to a operational amplifier (op amp) 352. The voltage drop across the transistor is normally 0.5 V. However, variations in Tx cause the voltage drop to vary and thereby impose a FSK AC signal on the loop voltage.

20       The filter 350 also receives a voltage corresponding to the loop current (i.e., the voltage across the resistor 320). The filter 350 uses this voltage to maintain the impedance of the valve controller 105 such that the valve controller 105 presents the desired impedance.

A bypass circuit 360, which includes a capacitor 362 in series with the parallel combination of a resistor 364 and a diode 366, permits higher frequency components of the loop signal to bypass the converter 310. Diodes 368 are used in providing intrinsically safe operation.

25       A multiplexer 370 receives inputs from the pressure sensors 235, 240, as well as from a temperature sensor 372. The multiplexer selectively provides these inputs to a second channel of the A-to-D converter 326. A third channel of the A-to-D converter is connected to the position converter 210.

30       An LED driver circuit 380 drives a set of light emitting diodes (LEDs). The LEDs provide local indications of the operations being performed by the valve controller 105. For example, the LEDs can provide an indication that a value is being obtained from the pressure sensor 235.



An actual implementation of the valve controller circuitry is illustrated in the circuit diagrams of Figs. 5-10. Corresponding elements from Figs. 2 and 3 are indicated in the circuit diagrams.

Other embodiments are within the scope of the following claims.

5           What is claimed is:

[illegible]

1           1. A 4-20 mA input interface circuit for communicating with a two-wire loop, the  
2 interface circuit including:

3           a power extraction circuit connected to the two-wire loop and operable to generate a  
4 DC operating voltage for use in powering the interface circuit and a related device, the power  
5 extraction circuit including a DC-to-DC converter that generates the DC operating voltage as  
6 a voltage having a smaller magnitude than a voltage between the two wires of the two-wire  
7 loop;

8           a current sensor connected to the two-wire loop and operable to generate a measure of  
9 an analog current through the two-wire loop, the measure being used in controlling a device  
10 associated with the interface circuit; and

11           a digital communications circuit connected to the two-wire loop and operable to inject  
12 a digital transmission signal on to the two-wire loop and to extract a digital reception signal  
13 from the two-wire loop, the digital communications circuit including an impedance controller  
14 having an operational amplifier connected to control an impedance presented to the two-wire  
15 loop by the interface circuit.

1           2. The interface circuit of claim 1, wherein the impedance controller is operable to  
2 present a stable impedance to the two-wire loop for frequencies in a digital communications  
3 band.

1           3. The interface circuit of claim 2, wherein the impedance controller presents an  
2 impedance substantially less than the stable impedance for frequencies outside of the digital  
3 communications band.

1           4. The interface circuit of claim 2, wherein the stable impedance is between 200 and  
2 300 ohms.

1           5. The interface circuit of claim 4, wherein the stable impedance is 250 ohms.

1           6. The interface circuit of claim 2, wherein the digital communications band extends  
2 from 500 Hz to 10 kHz.

3

1           7. The interface circuit of claim 2, wherein the impedance controller is operable to  
2 inject the digital transmission signal without reducing the impedance substantially below the  
3 stable impedance.

1           8. The interface circuit of claim 1, wherein the impedance controller includes a filter  
2 connected to one or more inputs of the operational amplifier.

1           9. The interface circuit of claim 1, wherein the impedance controller is connected to  
2 receive an AC signal having a varying frequency, the varying frequency corresponding to  
3 digital content of the digital transmission signal.

1           10. A valve controller including:  
2 a 4-20 mA interface circuit having terminals for connection to a two-wire loop;  
3 a processor in data communication with the interface circuit and operable to generate  
4 a control signal for controlling a valve position; and  
5 a control device operable to control the valve position in response to the control  
6 signal from the processor;

7           wherein the 4-20 mA interface circuit comprises:  
8 a power extraction circuit connected to the two-wire loop and operable to  
9 generate a DC operating voltage for use in powering the interface circuit and the processor;  
10 a current sensor connected to the two-wire loop and operable to generate a  
11 measure of an analog current through the two-wire loop, the measure being used in  
12 controlling a device associated with the interface circuit; and  
13 a digital communications circuit connected to the two-wire loop and operable  
14 to inject a digital transmission signal on to the two-wire loop and to extract a digital reception  
15 signal from the two-wire loop, the digital communications circuit including an impedance  
16 controller having an operational amplifier connected to control an impedance presented to the  
17 two-wire loop by the interface circuit.

1           11. The valve controller of claim 10, wherein the control device comprises a current-  
2 to-pressure transducer.

1           12. The valve controller of claim 10, wherein the power extraction circuit comprises  
2 a DC-to-DC converter that generates the DC operating voltage as a voltage having a smaller  
3 magnitude than a voltage between the two wires of the two-wire loop.

1           13. The valve controller of claim 10, wherein the impedance controller is operable to  
2 present a stable impedance to the two-wire loop for frequencies in a digital communications  
3 band.

1           14. The interface circuit of claim 13, wherein the impedance controller presents an  
2 impedance substantially less than the stable impedance for frequencies outside of the digital  
3 communications band.

1           15. The interface circuit of claim 13, wherein the stable impedance is between 200  
2 and 300 ohms.

1           16. The interface circuit of claim 15, wherein the stable impedance is 250 ohms.

1           17. The interface circuit of claim 13, wherein the digital communications band  
2 extends from 500 Hz to 10 kHz.

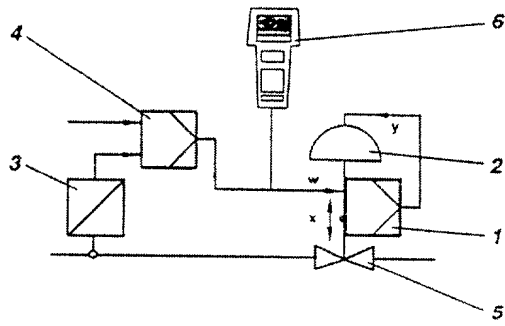
1           18. The interface circuit of claim 13, wherein the impedance controller is operable to  
2 inject the digital transmission signal without reducing the impedance substantially below the  
3 stable impedance.

1           19. The interface circuit of claim 12, wherein the impedance controller includes a  
2 filter connected to one or more inputs of the operational amplifier.

1           20. The interface circuit of claim 10, wherein the impedance controller is connected  
2 to receive an AC signal having a varying frequency, the varying frequency corresponding to  
3 digital content of the digital transmission signal.

## ABSTRACT

A 4-20 mA interface circuit for use, for example, in a valve controller, communicates with a two-wire loop. The interface circuit includes a power extraction circuit connected to the two-wire loop and operable to generate a DC operating voltage for use in powering the interface circuit and a related device, the power extraction circuit including a DC-to-DC converter that generates the DC operating voltage as a voltage having a smaller magnitude than a voltage between the two wires of the two-wire loop. The circuit also includes a current sensor connected to the two-wire loop and operable to generate a measure of an analog current through the two-wire loop, the measure being used in controlling a device associated with the interface circuit, and a digital communications circuit connected to the two-wire loop. The digital communications circuit is operable to inject a digital transmission signal on to the two-wire loop and to extract a digital reception signal from the two-wire loop. The digital communications circuit includes an impedance controller having an operational amplifier connected to control an impedance presented to the two-wire loop by the interface circuit.



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## 1.2 BLOCK DIAGRAM

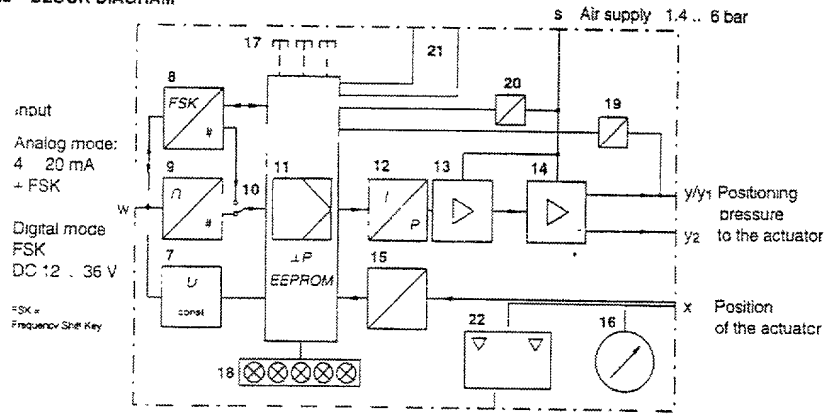


Fig. 1

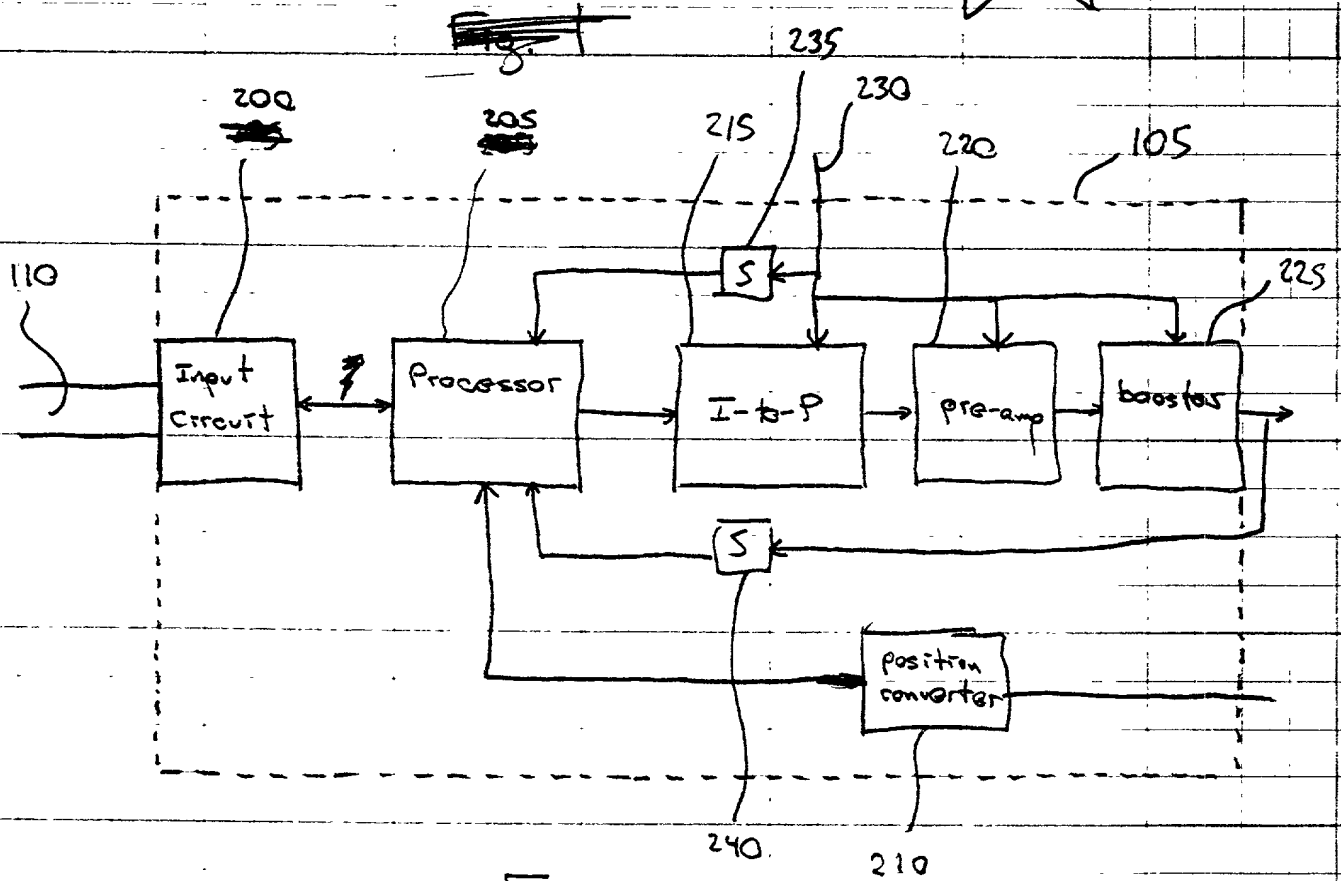
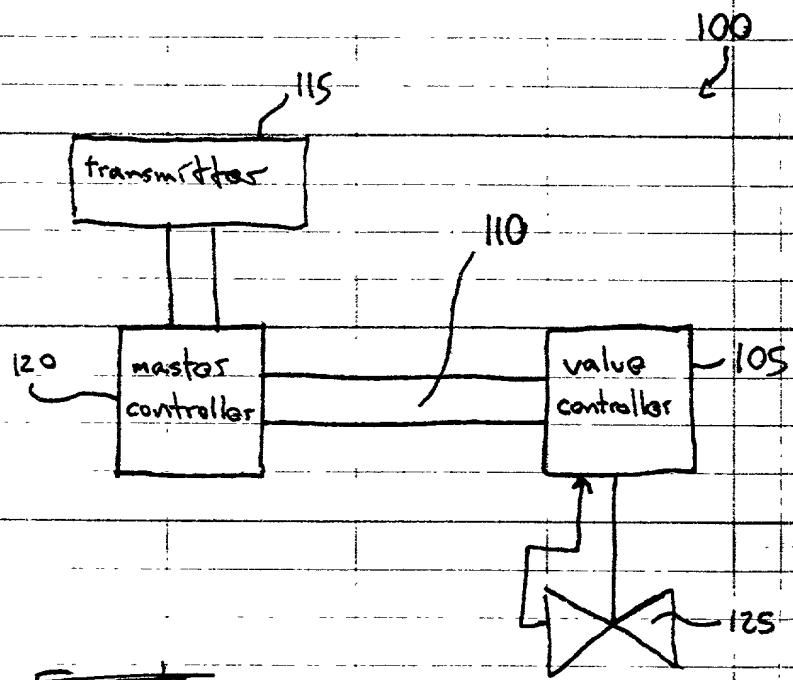
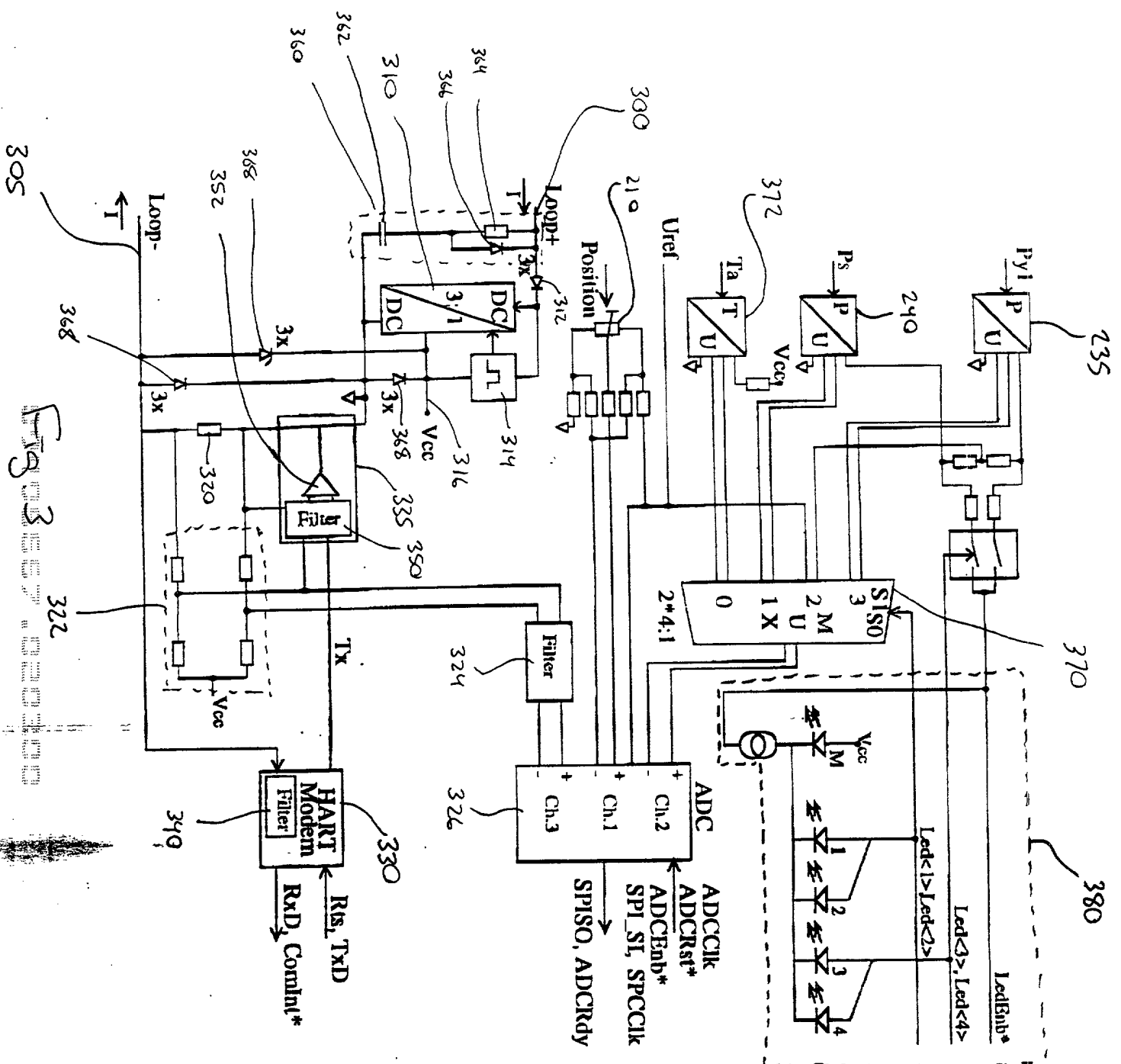


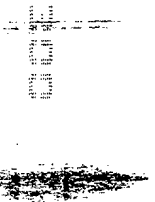
Fig. 2



305

Fig. 3

322



200



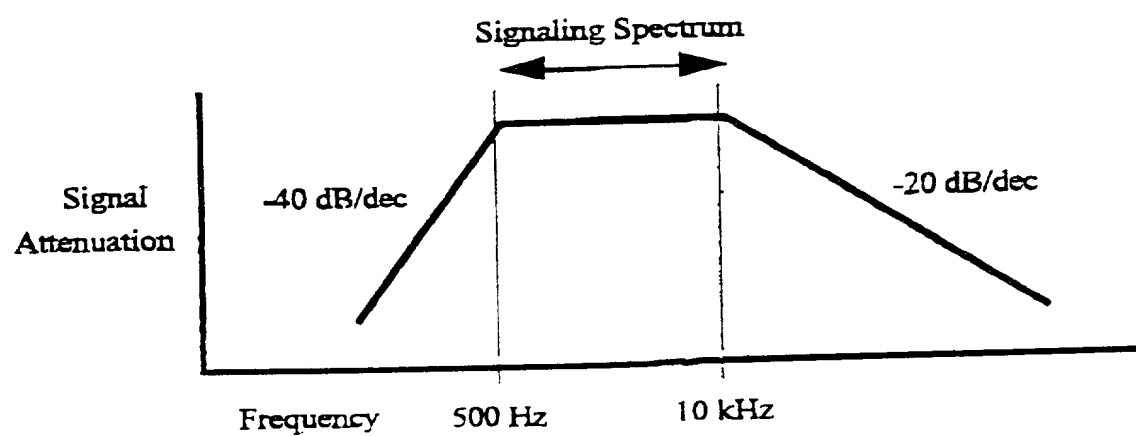


Fig. 4

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SRD91  
Intel1. Positioner, 4-20mA, HART, no options

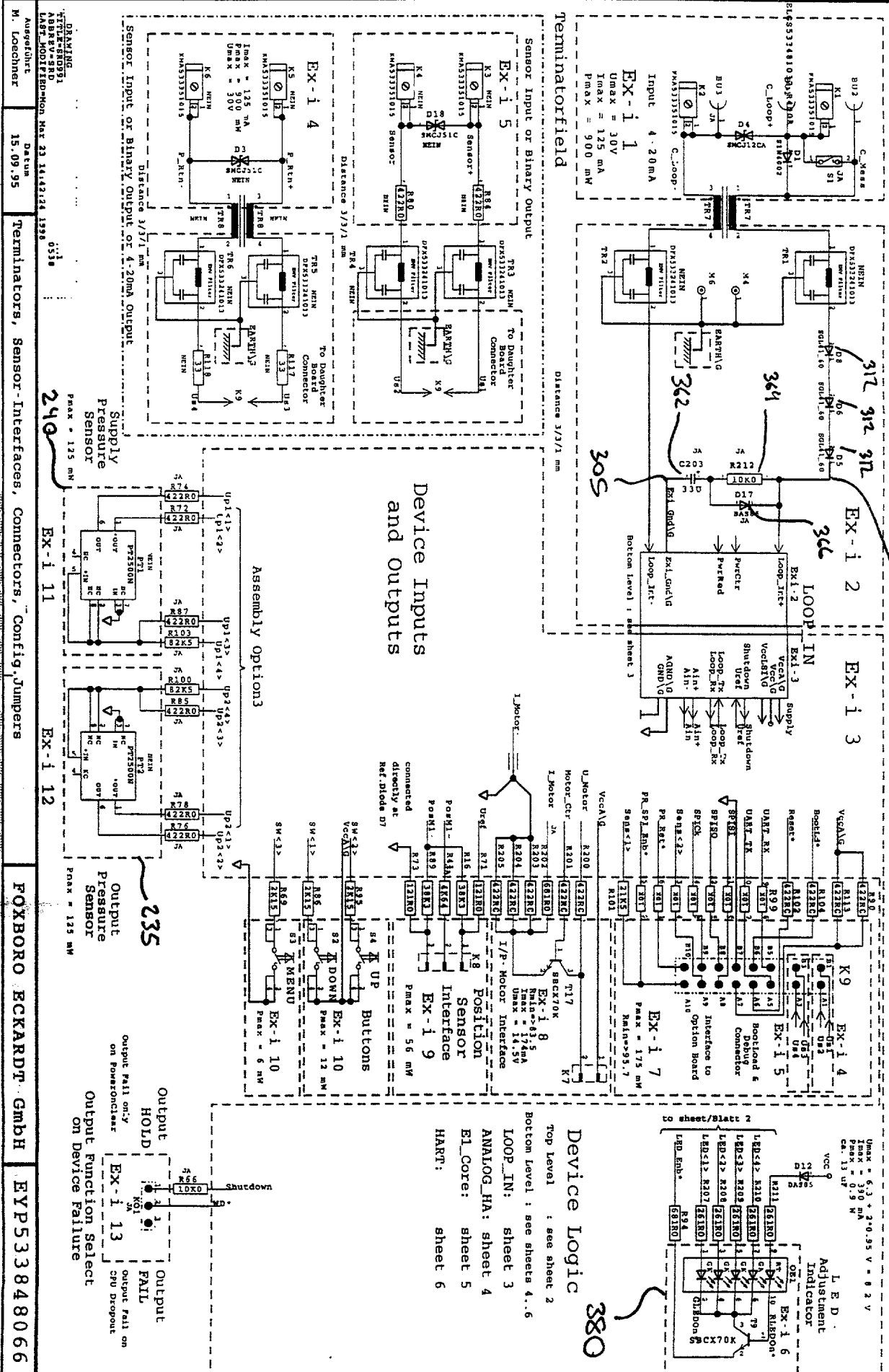
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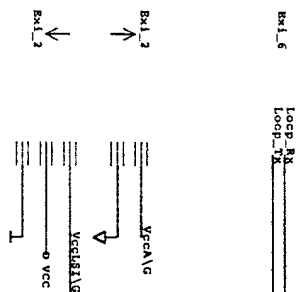
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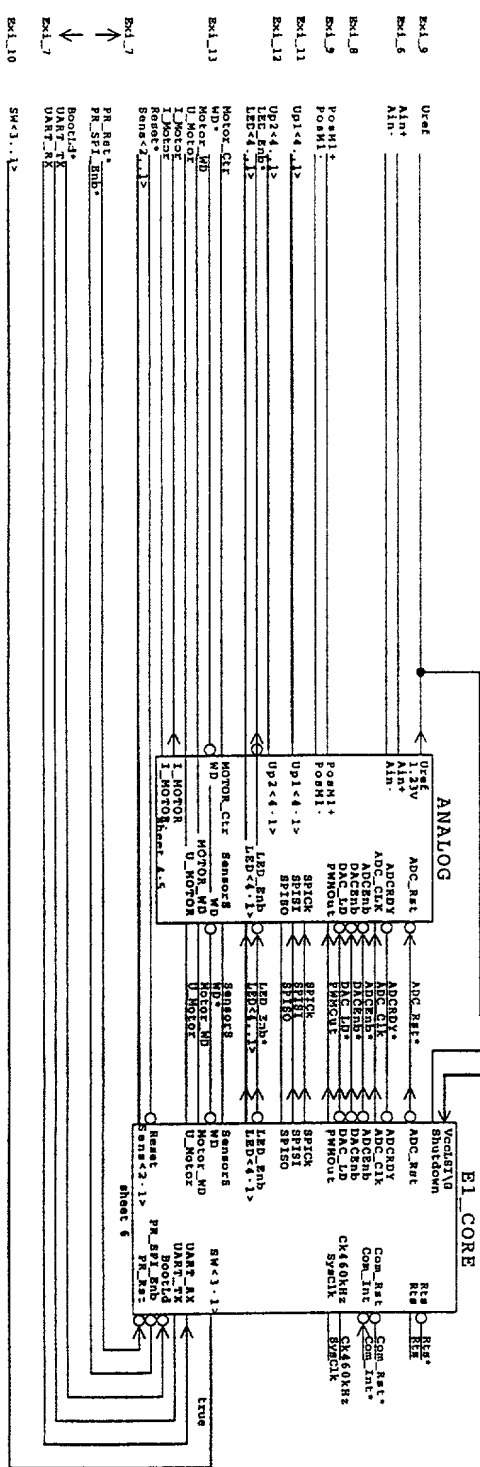
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Top Level of Core Electr., AD-Interface and Communication

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Fig. 6



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M. Loechner	15.09.95

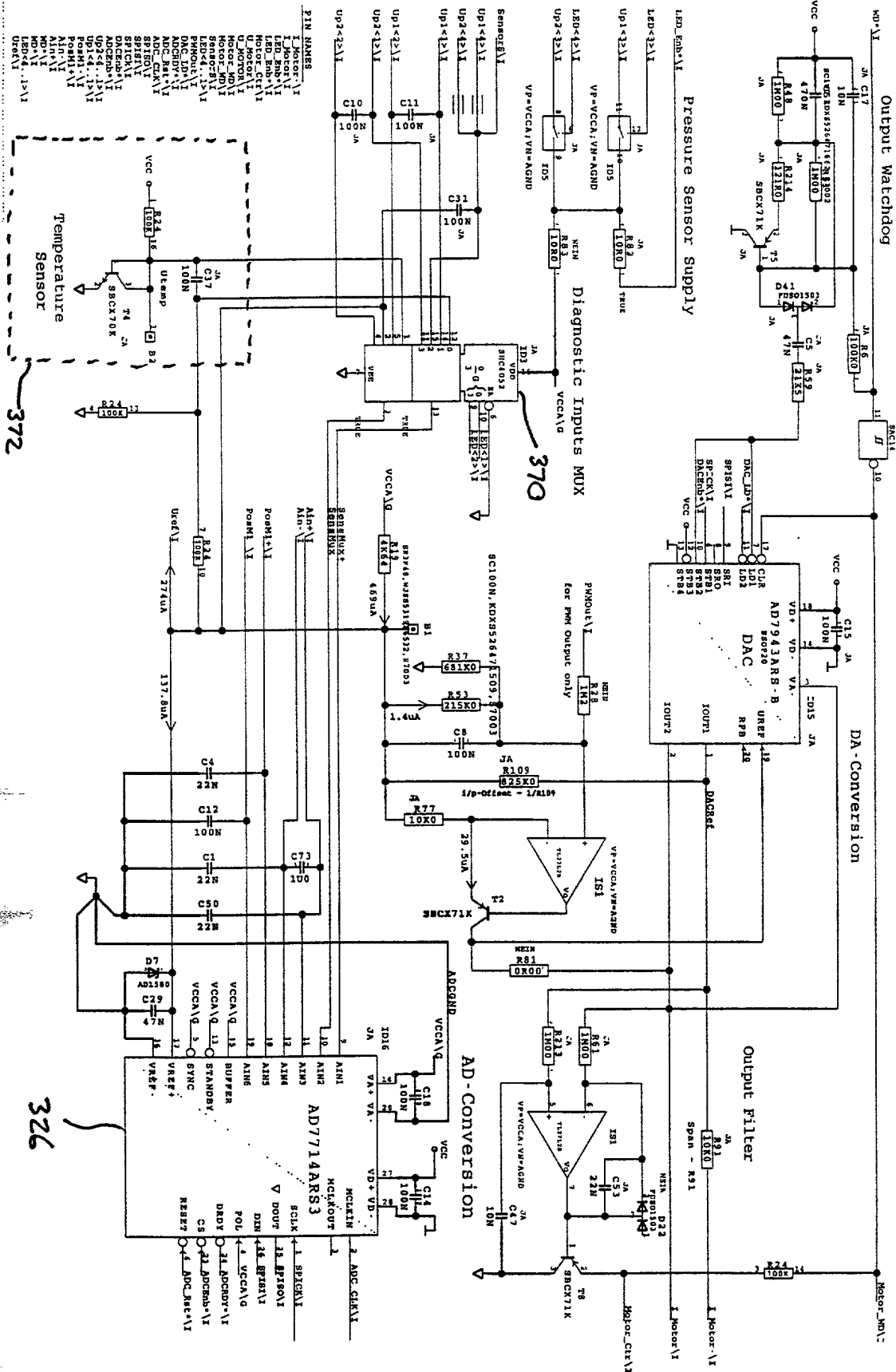
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AD -

## AD- and DA-Conversion, Diagnostic and Sensor Inputs

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**EYP533848066**

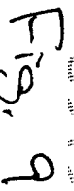


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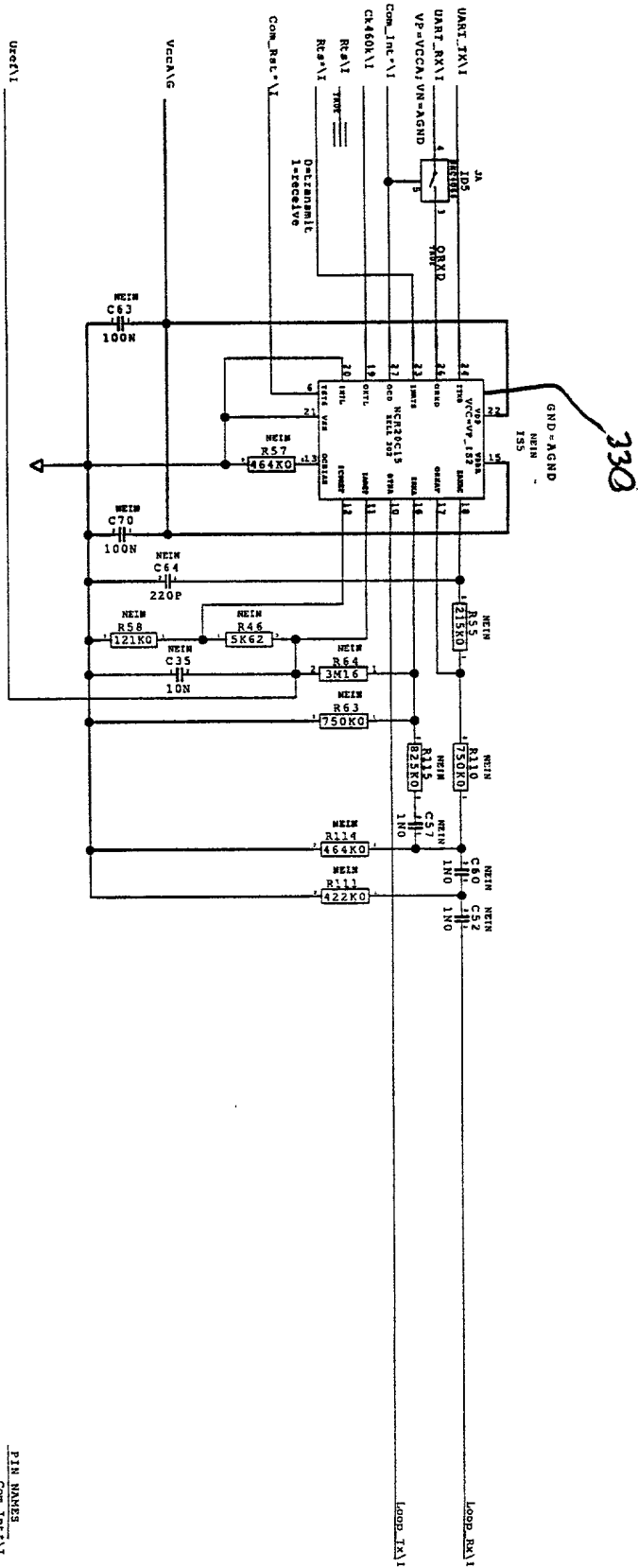
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SRD991  
Intel.Stellungsregler, 4-20mA, mit HART Komm.



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Rts\I      .....
Syc#Ck\I   .....
Shutdown\I .....
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## Communication Interface HART with "Filter," Encoder/Decoder